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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,766	10/02/2003	Eva Tois	SEPP21.001C1	1629

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,766	TOIS ET AL.	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/23/2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-9, 11-18, and 21-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over George et al ("Surface Chemistry for Atomic Layer Growth") in view of Suntola et al (US 6,015,590) and Sandhu et al (US 6,313,035).

George et al discloses a method of atomic layer growth of SiO_2 using $SiCl_4$ and H_2O in an atomic layer epitaxial method. George et al also discloses deposition of other oxides such as Al_2O_3, SnO_2, TiO_2, ZrO_2, In_2O_3, and HfO_2 (pg 13122). George et al also discloses The surface functional groups also provide the technical means to alternate between various materials with atomic layer control and form superlattices (pg 13131), this reads on applicants' multicomponent oxide thin film. George et al discloses repeating A and B reactions to form a desired layer (pg 13124), this reads on applicant's plurality of deposition cycles.

George et al does not disclose a multicomponent thin film comprising silicon and a transitional metal. George et al discloses ALE for a variety of oxide materials including SiO_2 and Al_2O_3, SnO_2, TiO_2, ZrO_2, In_2O_3, and HfO_2.

In a method of forming a multicomponent oxide layer, note entire reference, Sandhu et al teaches a multi-component oxide layer comprises a mixture of a metal oxide and silicon oxide, specifically a silicon oxide and titanium oxide (claims 1 and 3). Sandhu et al also teaches the multi-component layer may be formed using CVD and may also be deposited using other processes (Abstract). Sandhu et al teaches the titanium silicon oxide layer may be used in a memory cell, as a capacitor oxide or other semiconductor devices or structures (col 8, ln 1-35). Sandhu et also teaches other combinations of dielectric and metals can be used. (col 8, ln 1-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify George et al by selecting silicon dioxide and Al_2O_3, SnO_2, TiO_2, ZrO_2,

In_2O_3, or HfO_2 because a mixture of a metal oxide and a silicon oxide to form a useful multi-component oxide layer which can be used to manufacture a useful semiconductor device, as taught by Sandhu et al (col 8, ln 1-65).

The combination of George et al and Sandhu et al does not teach purging the reactor with an inert gas after each pulsing.

In a method of growing thin films using atomic layer epitaxy, Suntola et al teaches an interval between reactant pulses for evacuation of the entire gas volume in an apparatus during the interval between two successive reactant pulses and an inactive gas, this reads on applicant's inert gas, may be advantageously introduced to the reaction space during the evacuation (col 11, ln 20-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of George et al and Sandhu et al by purging the reactor with an inactive gas to prevent CVD film growth conditions, which are detrimental in an atomic layer epitaxy process (col 7, ln 50 to col 8, ln 20), as taught by Suntola et al.

Referring to claim 2, George et al teaches the growth rate is dependent on the number of reaction cycles (pg 13127), this reads on applicant's process is repeated to form a layer of a desired thickness.

Referring to claim 3-7, George et al teaches using $SiCl_4$, $HfCl_4$ and H_2O as reactants (pg 13122).

Referring to claim 8-9, George et al teaches deposition at 600 K (~327°C) (pg 13123).

Referring to claim 11-12, George et al teaches groove material with flat portions (Figure 1).

Referring to claim 13, George et al teach the deposition of dielectric films on trench or stacked capacitors for DRAM high storage memory (pg 13130) and Sandhu et al teaches forming a variety of semiconductor devices (col 8, ln 20-30); therefore forming on an electrode to form a semiconductor device would have been obvious to one of ordinary skill in the art.

Referring to claim 14-15, George et al teaches a superlattice structure formed by alternating various materials, which include HfO_2, TiO_2, Al_2O_3 and ZrO_2 (pg 13122 and 13131).

Referring to claim 16-18, George et al teaches SiO_2 gate oxides in MOSFET devices (pg 13121 col 1), deposition on a silicon surface (pg 13123 col 1) and the deposition higher dielectric gate oxide materials, such as TiO_2 and Al_2O_3 (pg 13130 col 2).

Referring to claim 22, the combination of George et al, Sandhu et al and Suntola et al teaches forming silicon oxide by pulsing a silicon compound followed by H_2O, forming a metal compound by pulsing a metal compound followed by H_2O (pg 13122) and purging the reactor between reactant pulses ('590 col 11, ln 30-40) to form a superlattice of various materials (pg 13131).

Referring to claim 24, the combination of George et al, Sandhu et al and Suntola et al teach self-limiting reactions (George et al Abstract).

4. Claims 1-9 and 11-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over George et al ("Surface Chemistry for Atomic Layer Growth") in view of Suntola et al (US 6,015,590) and Sandhu et al (US 6,313,035) as applied to claims 1-9, 11-18, and 21-33 above, and further in view of Suntola ("Atomic Layer Epitaxy").

The combination of George et al, Sandhu et al and Suntola et al ('590) teach all of the limitations of claim 19, as discussed previously, except the ratio of silicon compound contacting steps to metal compound contacting steps.

In a method of atomic layer epitaxy, Suntola teaches controlled growth of one atomic layer at a time is an ideal opportunity for making layered superalloys and superlattice structures. Suntola also teaches an ordered superalloy structure can be made by alternate sequencing of components and ratios other than 1:1 of the alternating component can be achieved by proportional sequencing or proportional dosing (4.2.3 Heterostructures of III-V compounds, pg 296-297). Suntola also teaches an A_1A_2B superalloy and a $(A_1B_1)_1(A_2B_2)_1$ superlattice (Fig 23). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of George et al, Sandhu et al and Suntola et al ('590) by using a 1:1 ratio because conventional superlattices contain a 1:1 ratio, as taught by Suntola.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over George et al ("Surface Chemistry for Atomic Layer Growth") in view of Suntola et al (US 6,015,590) and Sandhu et al (US 6,313,035) as applied to claims 1-9, 11-18, and 21-33 above, and further in view of Lowrey et al (US 5,891,744).

The combination of George et al, Sandhu et al and Suntola et al teach all of the limitations of claim 10, as discussed previously, except the thin multicomponent oxide is formed on a hemispherical grain structure.

In a method of monitoring the effects of hemispherical grains, Lowrey et al teach the capacitance of a polysilicon layer can be increased by increasing surface roughness of the

polysilicon film and one type of polysilicon film, which maximizes a roughness of an outer surface is hemispherical grain polysilicon (col 1, ln 10-67). Lowery et al also teaches deposition of a dielectric on a hemispherical grain area, which forms a capacitor (col 4, ln 1-15).

The combination of George et al, Sandhu et al and Suntola et al teach the deposition of dielectric films on trench or stacked capacitors for DRAM high storage memory (George pg 13130 col 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of George et al, Sandhu et al and Suntola et al by deposition the dielectric layer on a substrate having a hemispherical grain, as taught by Lowery et al, to enhance the capacitance of the capacitor.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over George et al ("Surface Chemistry for Atomic Layer Growth") in view of Suntola et al (US 6,015,590) and Sandhu et al (US 6,313,035) and further in view of Suntola ("Atomic Layer Epitaxy"), as applied to claims 1-9 and 11-33, and further in view of Lowrey et al (US 5,891,744).

The combination of George et al, Sandhu et al, Suntola et al ('590) and Suntola teach all of the limitations of claim 10, as discussed previously, except the thin multicomponent oxide is formed on a hemispherical grain structure.

In a method of monitoring the effects of hemispherical grains, Lowrey et al teach the capacitance of a polysilicon layer can be increased by increasing surface roughness of the polysilicon film and one type of polysilicon film, which maximizes a roughness of an outer surface is hemispherical grain polysilicon (col 1, ln 10-67). Lowery et al also teaches deposition of a dielectric on a hemispherical grain area, which forms a capacitor (col 4, ln 1-15).

The combination of George et al, Sandhu et al, Suntola et al ('590) and Suntola teach the deposition of dielectric films on trench or stacked capacitors for DRAM high storage memory (George pg 13130 col 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of George et al, Sandhu et al, Suntola et al ('590) and Suntola by deposition the dielectric layer on a substrate having a hemispherical grain, as taught by Lowery et al, to enhance the capacitance of the capacitor.

Response to Arguments

7. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 1/23/2006 have been fully considered but they are not persuasive.

Applicant's argument that George does not teach or suggest a multicomponent oxide film is noted but is not found persuasive. George teaches and suggests forming a superllatices, which suggests for a multicomponent oxide film. Superlattice are formed from alternating two different materials and the lattice is formed from a first atomic layer, then bonding a second layer completing a binary half reaction to form, for example silicon oxide, then a third layer is bonded to the second layer followed by a fourth material, for example titanium oxide. The first three layers reads on applicant's multicomponent oxide because silicon and titanium are bonded to the second layer.

Applicant's argument that no secondary reference suggest a dielectric layer of more then one type of metal oxide is noted but is not found persuasive. Sandhu et al teaches and suggests for a multicomponent oxide (Abstract).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJS
March 28, 2006

Matthew J Song
Examiner
Art Unit 1722

ROBERT KUNEMUND
PRIMARY EXAMINER